PERFORMANCE EVALUATION OF A THREE PHASE FIVE LEVEL MULTI-LEVEL INVERTER

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ABSTRACT

A novel three-phase five-level H-NPC Inverter was proposed in this paper. The proposed research involves developing a model of the inverter with number of power switches (IGBT) and four diodes per phase in order to achieve a three-phase five-level, output voltage waveform in a MATLAB/Simulink environment. The output line-to-line voltage is improved and the total harmonic distortion is lower than the conventional three-phase five-level power inverters, this proposed three-phase five-level inverter can achieve higher output voltage levels with these fewer components. The details analyses and mode of control schemes using Sinusoidal pulse width modulation were simulated base on the two performance matrices: Enhancing the voltage quality and mitigating the THD at the inverter output.

1. INTRODUCTION:

There is a growing interest in the need of Multilevel inverters in the area of the renewable energy system, grid energy connection and industries in recent years this is due to the higher demand of energy for higher and medium voltage control. These demand in energy and environmental consciousness have re-evoked human interest on the need of these inverters [1]. The inverter output is generated by synthesize a stepped waveform, which is which was made by selecting different voltage steps generated by properly connection of different capacitors as a voltage sources [2]. This connection was performed by the proper switching of the power switches (IGBT's and Diods). The number of levels assign to the converter can be defined as the number constant voltage values and that can be generated by the inverter between the output terminal and any internal reference node within the converter [3]. Typically, this is called dc-link node, denoted by N and called neutral.
The circuits of Fig. 1.0 illustrate the examples of this neutral connection.

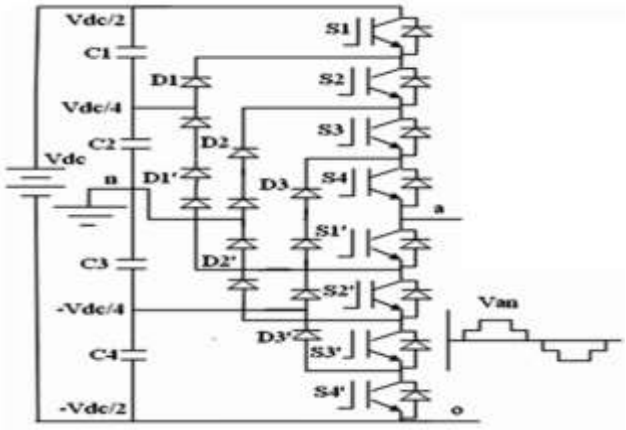

Fig 1.0 Single Phase Five Level Diode Clamp Inverter.

For the inverter to be called a multilevel inverter, the phases of the inverter have to generate at least three different voltage levels (+*Vdc*, 0 and -*Vdc*); this is what made it different from the conventional two-level voltage source inverters (2L-VSC.
Some of the single-phase examples of this inverters their respective waveforms are illustrated in Fig 1.1. The two-level inverter shown in Fig.1.1(a) generates an output voltage of positive or negative ±*Vdc*. It operate at a high switching frequencies along with SPWM technique making it to generate some voltages or current output waveform that has large number of harmonic contents, [4] [5]. Higher

rating of Semiconductor device and losses generated as a result of switching make a conversional two-level voltage source inverter less acceptable in a high power and high voltage applications.

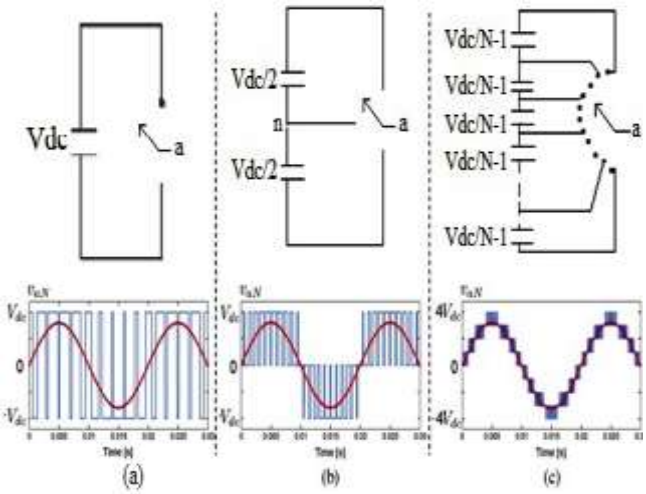

Fig. 1.1 Single phase Inverters and their output voltage waveform
(a) "two level", (b) "Three level". (c) "N-levels" [6], [5]

The topologies of a multilevel inverter, as shown in Fig. 1.1(b) and (c) make the system easier to attain higher voltage and power without stress the switches [7]. Higher voltage output waveform was generated from the addition of the capacitor voltage through the commutation of the switching devices, as shown in Fig. 1.1(c).

The input source of the inverter was formed from the series-connected capacitors, which also provide some nodes that the inverter can be connected to [7]. However, increase in a high number of levels increases complexity in controlling the system and introduces voltage unbalance problems: consequently, practical cost-effective and flexible control strategies are vital to the connection of these devices for renewable energy and the grid connected systems, as well as industrial application of these multilevel inverters [8]. Often the above advantages, various circuit topologies and modulation strategies were developed for better utilization of the voltage source inverters. Some of The re-now topologies reported in a literatures are: Neutral Point Clamp (NPC) inverters discovered by [9], the flying Capacitor (FC) Developed by [2], and the Cascaded Hybrid Inverter (CHI) called H-bridge inverters [10]. The three-level NPC inverter has some level of acceptance due to its fewer number of switches and capacitors, low device count [3]. Even though higher number of levels could be achieved by extending the NPC structure, but unbalance voltage of the DC-link capacitors and uneven distribution of losses in the inner and outer devices make it less attractive.

An improve model of the NPC Inverter called H-bridge / Neutral Point Clamped (H-NPC) inverter were introduced, the topology retains the structure of NPC inverter in H-bridge form which allows it to generate the output voltage waveform and solves the problem of unbalancing voltage cause by increase in the higher number of levels in NPC inverter.

2. Proposed multilevel Inverter Modeling and its Operation

The proposed Five-level H-NPC inverter consists "two" three-level NPC inverter with the phase leg of each cell sharing a common DC bus, as indicated in Fig.1.0.

combining three step voltage levels of each of these two connected legs result a 5-level voltage waveform. Each of leg hes has four switching devices with four freewheeling diodes and two clamping diodes in order to clamp the switches to the neutral. The topology has an advantage of generating five step voltage levels in its phase voltages *Van*, *Vbn* and *Vcn* when compared to the three levels for NPC inverter, this result in the low THD [4]

The overall voltage stress on all the switching devices (eight in No) is half of DC bus voltage. While the phase voltage of the inverter is the difference between the two legs voltage as stated in Equation (1) [11].

$$V_{an} = V_1 - V_2 \quad (1)$$

Meanwhile, the waveform of phase voltage V_{an} is formed with five voltage levels .[11, 12].

$+V_{dc}$, $+V_{dc}/2$, 0, $-V_{dc}/2$ and $-V_{dc}$

From each phase of this multilevel inverter, the eight number of switches contribute to make four complementary switch pairs: (S_{11}, S_{13}), (S_{12}, S_{14}), (S_{21}, S_{23}) and (S_{22}, S_{24}) as in the case of phase 'a' shown in Fig.1.0

Consequently, four independent gate signals are required to form the modulation scheme for the top four and bottom switches respectively.

The other phase voltages; V_{bn} and V_{cn} from the circuit of Fig 1.0, are produced in the same manner as in phase 'a' with phase angle shift of 120° and 240° in their modulating signals respectively.

The line voltage is produced from the difference of two phase voltages as given in Equation (2.1), and it will contain nine voltage levels

$+2V_{dc}, +3V_{dc}/2, +V_{dc}, +V_{dc}/2$, 0, $-V_{dc}/2$, $-V_{dc}$, $-3V_{dc}/2$ and $-2V_{dc}$.

$V_{ab} = V_{an} - V_b$ [11] (2)

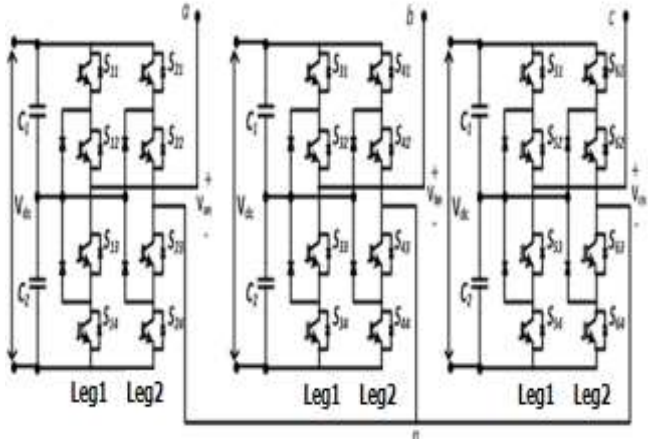

Fig.2.0 Three Phase Five Levels H-NPC Inverter Circuit Diagram [13]

The switching operation of H-NPC inverter of Fig 1.0 is based on that of the phase leg of a three-level NPC inverter, were referring to phase 'a' switching ON the upper switches (S_{11} and S_{12}) in each leg produces $V_{dc}/2$.

Switching ON the middle switches (S_{12} and S_{13}) produces zero voltage.

When swathing ON the Lower switches (S_{13} and S_{14}) $-V_{dc}/2$ voltage produces. The phase voltage of H-NPC inverter produces five voltage levels, $V_{dc,}\, V_{dc}/2, 0, -V_{dc}/2$ and $-V_{dc}$ when the dc bus voltage is $V_{dc}/2$.

3. Proposed Multicarrier SPWM Techniques

Power electronics inverters are operating in a "switched mode", meaning that the inverter switches are either in the ON state (saturated with only a small voltage drop across the switch) or turn- OFF state (no current flows).
In power electronics inverters Modulation is defined as the switching process of semiconductor switches between ON and OFF state. When the switches alternate between these two states, the flow of power in the inverter can be control.

Controlling the output voltage waveform in multilevel inverters employ deferent techniques, the control techniques are classified mainly based on the switching frequencies from either low or high [8, 13]

The Sinusoidal Pulse Width Modulation (SPWM) is one of the most effective control scheme used in driving the inverters.
In principle, SPWM generates the control pulses by comparing a triangular carrier waveform and a sinusoidal reference waveform base on equation 3.0
In all this modulating process a maximum attenuation of the switching component is required. However, the switching frequency fc called the carrier frequency and peak to peak amplitude of *A*c should be many times higher than the frequency of the desired fundamental AC component (sinusoidal modulation signal) fr, and peak-to-peak amplitude of Ar seen at the input or output terminals.

Switching frequency of the inverter and the high order harmonic component of the output voltage is normally defines by the frequency of the carrier signals [14].

Making the inverter output frequency and voltage adjustable and eliminating lower order harmonics is the main purposed of SPWM.

A simple Circuit diagram and SPWM for single- phase two-level voltage source inverter with the semiconductor switches represented by an ideal switch is shown in Fig. 3.0(a) while Fig 3.0(b) shows the carrier and modulating

waveform with the respective pulse generated at the output.

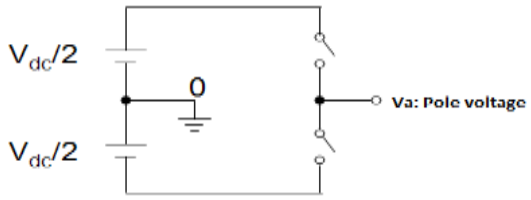

Fig. 3.0(a) Circuit Diagram for Single Phase Two Level Voltage Source Inverter [6]

At the point of the intersection between the carrier and modulating signals the inverter output voltage: $V_{a0} = V_{dc/2}$,When $V_{control} > V_{triangle}$ and

$V_{a0} = -V_{dc/2}$, When $V_{control} < V_{triangle}$

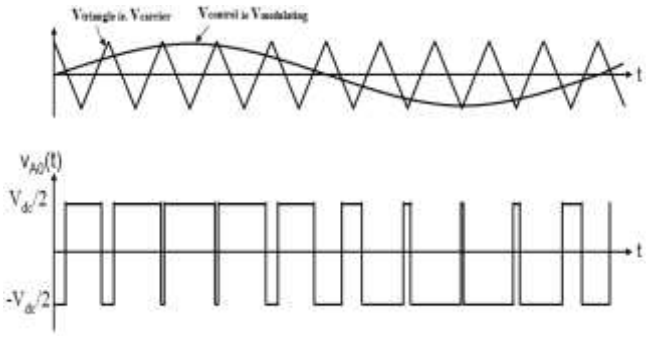

Fig 3.0(b). SPWM Output Waveform for Single Phase Two Level Voltage Source Inverter [6]

The amplitude of the signal is controlled by the peak value of $V_{control}$ and Fundamental frequency is controlled by the frequency of $V_{control}$ while keeping amplitude and frequency of carrier fixed. Modulation Index 'M' is given by:

$$M = \frac{V_{control}}{V_{triangle}} \text{ [8, 15].} \quad (3)$$

Where: $V_{control}$ and $V_{triangle}$ are the modulating and carrier voltages signals respectively.

In a three-phase multilevel voltage inverter control, all the carrier signals are compared with the reference waveform to generate a pulse of signal for a particular complementary pair of switches in a particular cell of multi-cell inverter, this generated string of pulses is used to control the power switches. The active power switch is ON when the reference waveform is greater than the carrier signal associated with that switch. As the number of levels increases in the multilevel inverter, the switching devices required increases. For example, for a five-level diode clamped multilevel inverter of one leg, the switching devices used are 8, 4 for the positive half cycle and other 4 for the negative half cycle. So, one sine wave is compared with a four-triangular wave and each one's compared output is given to the each switching devices. For the next leg, these waves are shifted 120° and the same for the third leg [8, 15].

4. Set up for the Simulation Model

The simulation of 5-level NPC inverter involves building the MATLAB/Simulink model of these inverter circuits, as described in section 2.0.

The internal parameters of switching devices (IGBT and diodes) were given as: Load Voltage Frequency 50 Hz, Switching Frequency 7.5 KHz, C1& C2 1 mF DC Voltage 150 V as obtained in a datasheet

The Simulation models for SPWM was developed according to the orientation of their reference and carrier signals. However, the modulating index m_a was chosen in the range of 0.2 – 1.0, so as to have several values of the performance criteria [Shehu, Shanono [16]]. Also, the carrier frequency was choosen as 7500 Hz, so as not to exceed the switching frequency limit of the switching device (IGBT). The MATLAB/Simulink blocks were shown in the following sections where the SPWM technique was connected to the inverter and run the simulation; two carrier signals were applied across the positive half cycle of the modulating signal, and other two signals were applied across the negative half cycle of the modulating signal.

Fig. 4.0 illustrated the arrangement of carrier modulation signals of a 5-level inverter.

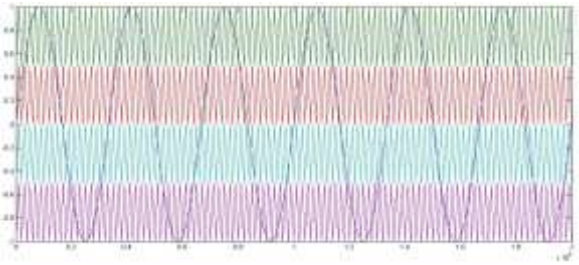

Fig. 4.0 arrangement of carrier modulation signals of 5-level inverter

Eight PWM signals were generated from this signal and then serve the eight switches of a leg of the inverter of circuit Fig. 4.1

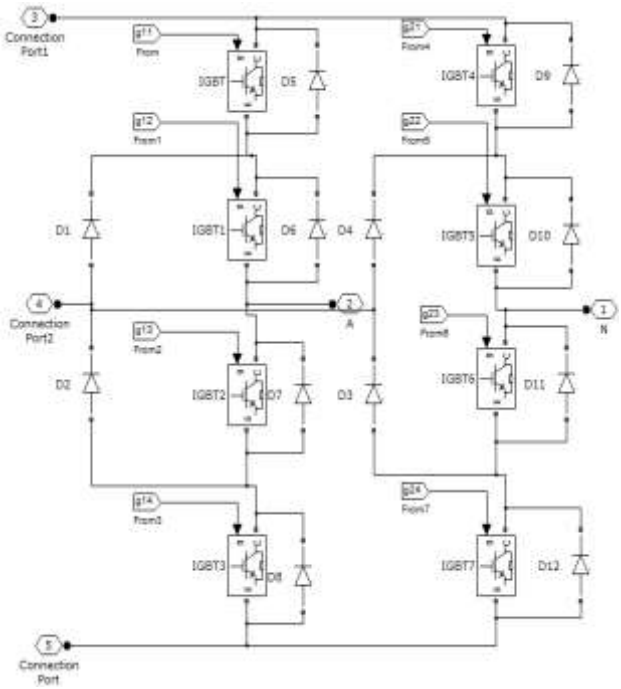

Fig. 4.1 Internal Circuitry of Phase 'a' Subsystem1 of 5 Level H-NPC Inverter

In the same manna, other pulses were generated for the remaining phases; with difference that the modulating signal shifted by 120 phase shift.

Fig. 4.2 is the model of a 5-level H-NPC inverter consisting of several subsystems. While Figs. 4.1 and 4.3 show the internal circuitry of subsystem1 of phase 'a' and SPWM simulation block of phase 'a', of 5-level H-NPC inverter respectively.

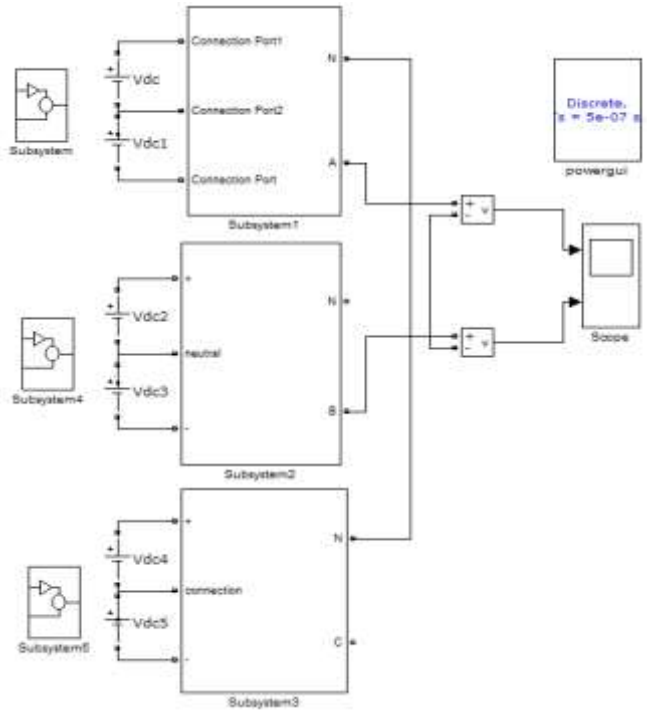

Fig 4.2 Three Phase 5-Level H-NPC Inverter Simulation Model

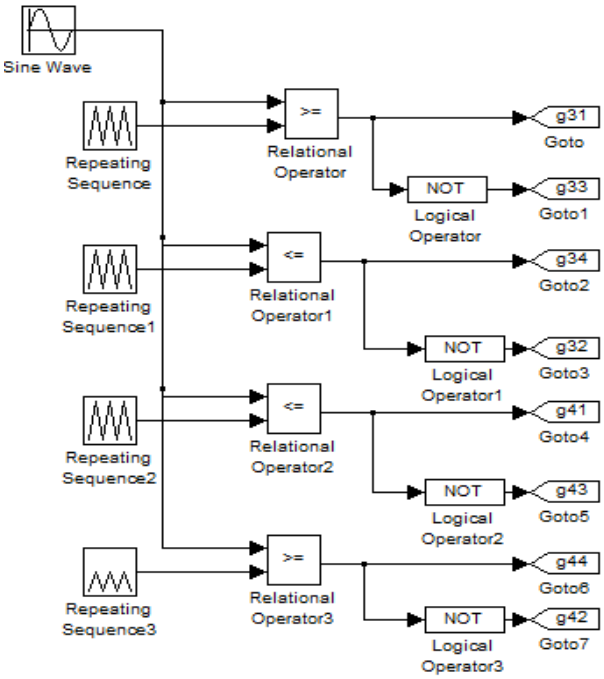

Fig 4.3 SPWM Simulation Block of 5-Level H-NPC Inverter in Phase 'a',

SPWM was applied to H-NPC inverter resulting in the switching of switching devices that produced the phase and line voltage. Throughout the simulation process we keep on varying the amplitude modulation index m_a in the range of 0.2 to 1.0.

Fig 4.4(a) depict the phase voltage waveform and its harmonic contents for $index\ of\ m_a = 0.2$. The line-line voltage waveform and its Harmonics contents were shown in Fig 4.4(b).

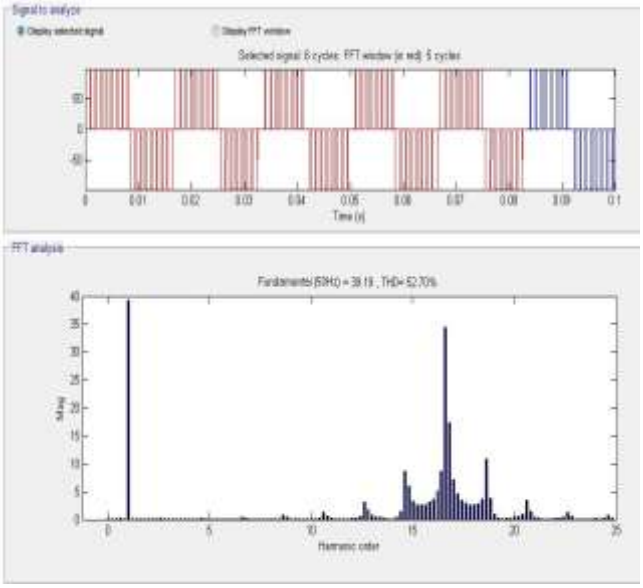

Fig 4.4(a): Phase Voltage Waveform and Harmonic Contents of 5-Level H-NPC Inverter at m_a = 0.2

The waveform of the phase voltage contains three voltage levels with THD of 52.70%. While the phase voltage was recorded to have 39.19 *V* as the magnitude of the peak value of the fundamental component and 27.17 *V* as its rms value. The THD has reduced to 41.90 % in the line voltage due to the three-phase balance system as the triple order harmonics cancel out between the phases. The simulation gives 67.78 *V* as the magnitude of the peak value of the fundamental component and 47.93
V rms value.

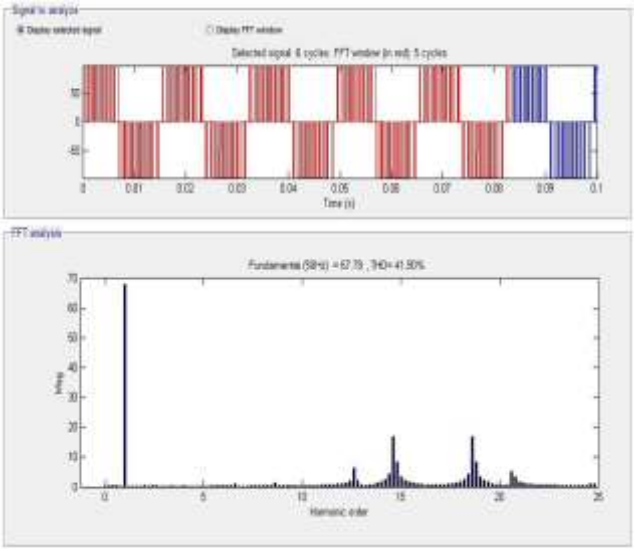

Fig 4.4 (b) Line Voltage Waveform and Harmonic Contents of 5-Level H-NPC Inverter at m_a = 0.2

for $m_a = 0.4$ the waveform and harmonic contents are similar to the one generated for $m_a = 0.2$ in which the waveform contains three voltage levels in phase waveform with 27.91 % as the THD, as shown in Fig 4.5(a). The phase voltage has 78.39 *V* as the magnitude of the peak value of the fundamental component and 55.43 *V* as its rms value.

The THD was reduced to 22.34 % in the line output voltage, as depicted in Fig 4.5(b) while the line voltage has 135.70 *V* as the magnitude of the peak value of the fundamental component and 95.98 *V* as its rms value.

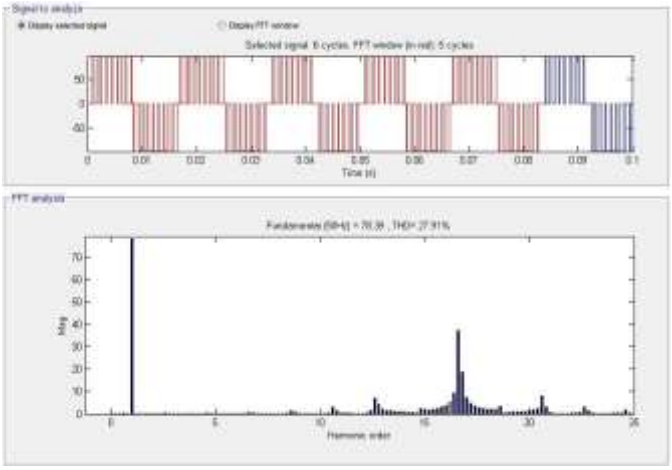

Fig 4.5(a): Phase Voltage Waveform and Harmonic Contents of 5-Level H-NPC Inverter at m_a = 0.4

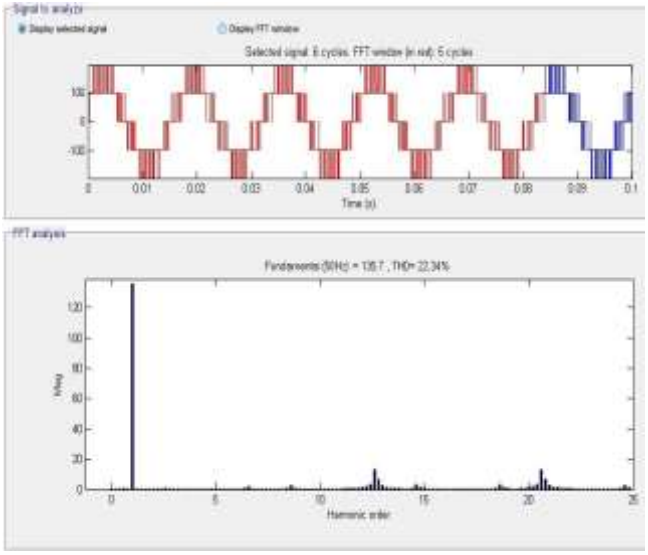

Fig 4.5(b) Line Voltages: Waveform and Harmonic Contents of 5-Level H-NPC Inverter at m_a =0.4

At $m_a = 0.6$, the phase voltage consists of five voltage levels with 18.65 % THD, as shown in Fig 4.6(a). The phase voltage has 117.7 *V* as the magnitude of the peak value of the fundamental component and 83.25 *V* as its rms value. The line voltage contains Seven voltage levels with 12.80 % THD, as depicted in Fig 4.6(b). The line voltage has 203.70 *V* as the magnitude of the peak value of the fundamental component and 144.10 *V* rms value.

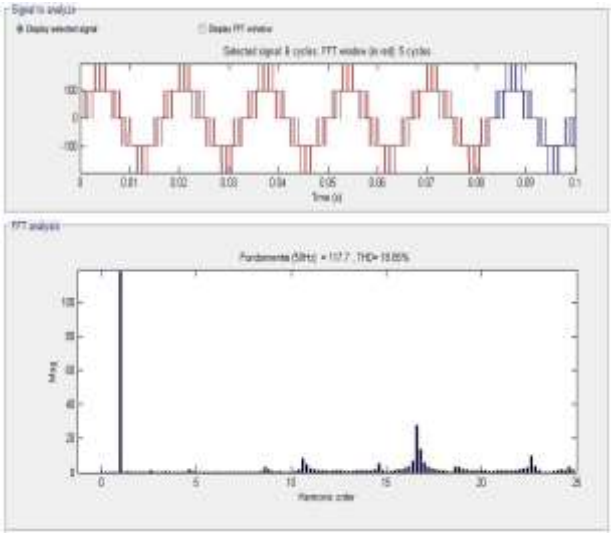

Fig 4.6 (a)Phase Voltage: Waveform and Harmonic Contents of 5-Level H-NPC Inverter for m_a = 0.6

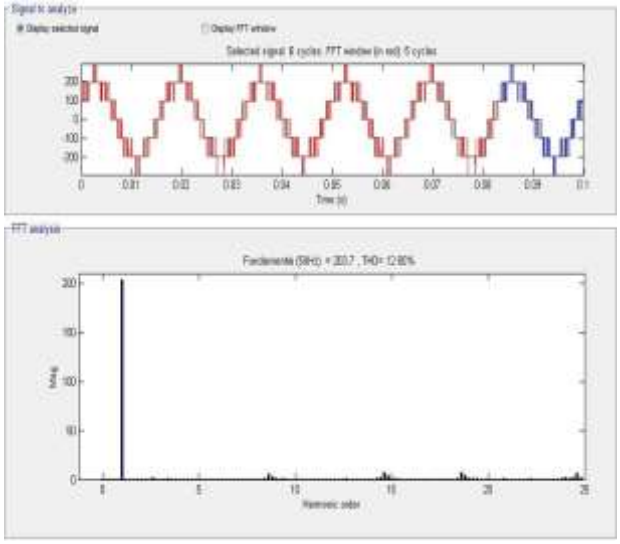

Fig 4.6(b) Line voltage: Waveform and harmonic contents of 5-level H-NPC inverter for
m_a = 0.6

For $m_a = 1.0$ the phase voltage consists of five voltage levels with 10.22 % THD, as shown in Fig 4.7(a). The phase voltage has 196 *V* as the magnitude of the peak value of the fundamental component and 162.00 *V* as its rms value. The line voltage contains nine voltage levels with 7.93 % THD as depicted in Fig 4.7(b). The line voltage has 339.5*V* as the magnitude of the peak value of the fundamental component and 256.00 *V* as its rms value.

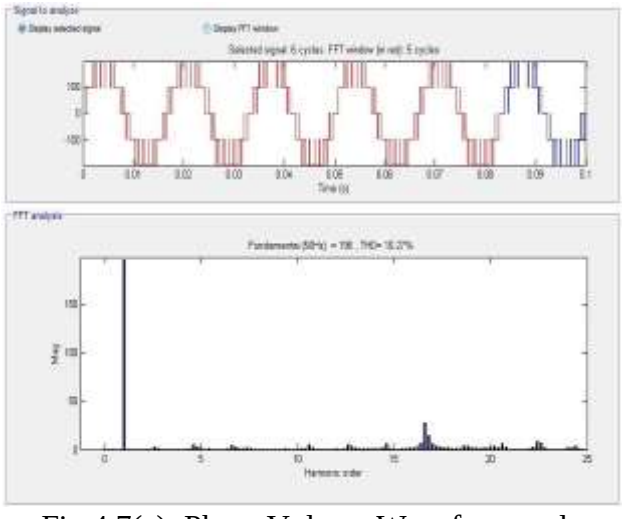

Fig 4.7(a): Phase Voltage Waveform and Harmonic Contents of 5-Level H-NPC Inverter for m_a = 1.0

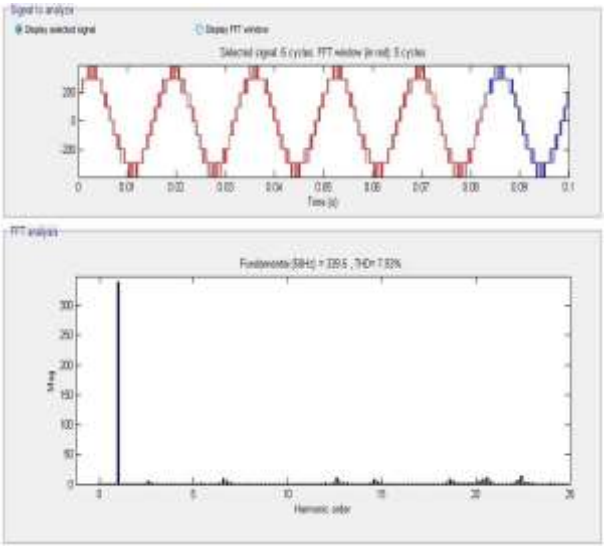

Fig 4.7(b) Line Voltage: Waveform and Harmonic Contents of 5-Level H-NPC Inverter at m_a = 1.0

Fig 4.2(a) and 4.3(a) shows that when the amplitude modulation index at and below 0.5 produces waveforms that contain three voltage levels in the phase voltage while above 0.5 produces five voltage levels as shown in Figs 4.5(a) and 4.6(b). Fig 4.7(b) shows that the line voltage consists of seven voltage levels at m_a =0.6. Fig 4.6(b) shows that the line voltage consists of seven voltage levels at m_a = 0.8. Table 4.0 shows changes in the THD, peak and rms value of the fundamental component with the variation of amplitude modulation index in the range of 0.2 to 1.0. The Total Harmonic Distortion decreases as the amplitude modulation index increases, as given in Table 1 Fig 4.7 shows the graphical representation of variation in THDs as amplitude modulation index varied from 0.2 to 1.0.

Table 4.0: Five Level H-NPC Simulation Results with variation in Amplitude Modulation Index

Amplitude Modulation Index m_a	Phase THD (%)	Phase peak value (V)	Phase rms value (V)	Line THD (%)	Line Peak value (V)	Line rms value (V)
0.2	52.70	39.19	27.17	41.90	67.78	47.93
0.4	27.19	78.39	55.43	22.34	135.70	95.98
0.6	18.65	117.70	83.25	12.80	203.70	144.10
0.8	14.90	156.90	11.1.0	11.61	217.50	192.00
1.0	10.27	196.00	138.60	7.93	339.50	240.10

TABLE 4.10 Comparisons of Simulation Results on THD with IEEE Standard 519-2014 Harmonics limit at 100% modulation index

IEEE std THD limit (%)	Simulation values from 5-level inverter (%)	Percentage improvement (%) On 5-level
8.00	7.93	0.88

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